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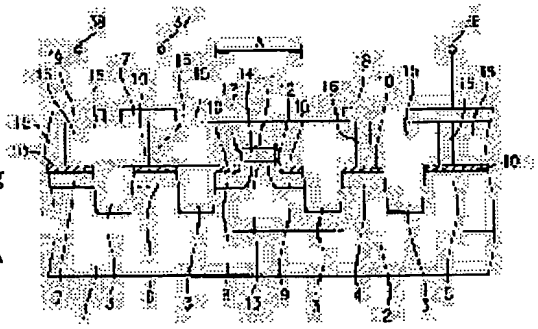
(54) ELECTROSTATIC PROTECTOR OF SEMICONDUCTOR INTEGRATED CIRCUIT, ITS MANUFACTURE, AND ELECTROSTATIC PROTECTION CIRCUIT USING THE ELECTROSTATIC PROTECTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To provide an electrostatic protector, its manufacturing method, and an electrostatic-protection circuit using the electrostatic protector which can be formed, without providing additionally any special process and photomask in its manufacturing process, even when using a salicide process.

SOLUTION: An electrostatic protector has a thyristor and a trigger diode A for triggering the thyristor at a low voltage to bring it into an on-state. The trigger diode A has an n-type heavily-doped cathode region 9, a p-type heavily-doped anode region 8. A gate oxide film 13 which is provided between the n-type heavily-doped cathode region 9 and the p-type heavily-doped anode region 8 and constitutes the gate of a MOS transistor of a semiconductor integrated circuit, a polysilicon 14 laminated on the gate oxide film 13, and gate sidewall insulators 12 formed on the sidewalls of the gate oxide film 13 and the polysilicon 14, which



insulate electrically the silicide layer formed on the surface of the n-type heavily-doped cathode region 9 from the silicide layer formed on the surface of the p-type heavily-doped anode region 8.

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CLAIMS

[Claim(s)]
[Claim 1] It is prepared in the input section or the output section of a semiconductor integrated circuit. It is electrostatic-protection equipment which protects the internal circuitry of this semiconductor integrated circuit from the inflow of the static electricity surge from the outside of this semiconductor integrated circuit to this semiconductor integrated circuit, or bleedoff of the static electricity surge to the exterior of this semiconductor integrated circuit to this semiconductor integrated circuit. It has the thyristor and the trigger diode which carries out the trigger of this thyristor to an ON state by the low battery. This trigger diode n mold cathode high concentration impurity range and p mold anode high concentration impurity range, Electrostatic-protection equipment equipped with an insulating means to insulate electrically the silicide layer formed in the front face of this n mold cathode high concentration impurity range, and the silicide layer formed in the front face of this p mold anode high concentration impurity range.
[Claim 2] The gate oxide which this insulating means is formed between this n mold cathode high concentration impurity range and this p mold anode high concentration impurity range, and forms the gate of the MOS transistor of this semiconductor integrated circuit, It is formed on this gate oxide at the side attachment wall of the polish recon by which patterning was carried out, and this gate oxide and this polish recon. Electrostatic-protection equipment containing the gate side-attachment-wall insulator with which the silicide layer formed in the front face of this n mold cathode high concentration impurity range and the silicide layer formed in the front face of this p mold anode high concentration impurity range are insulated electrically according to claim 1.
[Claim 3] This insulating means is electrostatic-protection equipment containing the isolation insulator which is formed between this n mold cathode high concentration impurity range and this p mold anode high concentration impurity range, and forms the component isolation region of the MOS transistor of this semiconductor integrated circuit according to claim 1.
[Claim 4] It is electrostatic-protection equipment according to claim 2 with which this electrostatic-protection equipment is formed in the p type semiconductor substrate, this n mold cathode high concentration impurity range is formed into n mold well, this a part of p mold anode high concentration impurity range is included in this n mold well, and these a part of other p mold anode high concentration impurity ranges are included in this p type semiconductor substrate or p mold well.
[Claim 5] It is electrostatic-protection equipment according to claim 2 with which this electrostatic-protection equipment is formed in the p type semiconductor substrate, this p mold anode high concentration impurity range is formed into this p type semiconductor substrate or p mold well, this a part of n mold cathode high concentration impurity range is included in n mold well, and these a part of other n mold cathode high concentration impurity ranges are included in this p type semiconductor substrate or this p mold well.
[Claim 6] It is electrostatic-protection equipment according to claim 2 with which this electrostatic-protection equipment is formed in the n-type-semiconductor substrate, this n mold cathode high concentration impurity range is formed into this n-type-semiconductor substrate, this a part of p mold

anode high concentration impurity range is included in p mold well, and these a part of other p mold anode high concentration impurity ranges are included in this n-type-semiconductor substrate or n mold well.

[Claim 7] It is electrostatic-protection equipment according to claim 2 with which this electrostatic-protection equipment is formed in the n-type-semiconductor substrate, this p mold anode high concentration impurity range is formed into p mold well, this a part of n mold cathode high concentration impurity range is included in this p mold well, and these a part of other n mold cathode high concentration impurity ranges are included in this n-type-semiconductor substrate or n mold well.

[Claim 8] It is electrostatic-protection equipment according to claim 3 with which this electrostatic-protection equipment is formed in the p type semiconductor substrate, this n mold cathode high concentration impurity range is formed into n mold well, this a part of p mold anode high concentration impurity range is included in this n mold well, and these a part of other p mold anode high concentration impurity ranges are included in this p type semiconductor substrate or p mold well.

[Claim 9] It is electrostatic-protection equipment according to claim 3 with which this electrostatic-protection equipment is formed in the p type semiconductor substrate, this p mold anode high concentration impurity range is formed into this p type semiconductor substrate or this p mold well, this a part of n mold cathode high concentration impurity range is included in n mold well, and these a part of other n mold cathode high concentration impurity ranges are included in this p type semiconductor substrate or p mold well.

[Claim 10] It is electrostatic-protection equipment according to claim 3 with which this electrostatic-protection equipment is formed in the n-type-semiconductor substrate, this n mold cathode high concentration impurity range is formed into this n-type-semiconductor substrate, this a part of p mold anode high concentration impurity range is included in p mold well, and these a part of other p mold anode high concentration impurity ranges are included in this n-type-semiconductor substrate or n mold well.

[Claim 11] It is electrostatic-protection equipment according to claim 3 with which this electrostatic-protection equipment is formed in the n-type-semiconductor substrate, this p mold anode high concentration impurity range is formed into p mold well, this a part of n mold cathode high concentration impurity range is included in this p mold well, and these a part of other n mold cathode high concentration impurity ranges are included in this n-type-semiconductor substrate or n mold well.

[Claim 12] The manufacture approach of the electrostatic-protection equipment which includes the insulating means formation process which forms an insulating means are the manufacture approach of electrostatic-protection equipment according to claim 1, and insulate electrically the process which forms n mold cathode high-concentration impurity range, the process which forms p mold anode high-concentration impurity range, and the silicide layer formed in the front face of this n mold cathode high-concentration impurity range and the silicide layer formed in the front face of this p mold anode high-concentration impurity range.

[Claim 13] The process which forms the gate oxide in which this insulating means formation process forms the gate of the MOS transistor of a semiconductor integrated circuit on a silicon substrate, The process which carries out patterning of the polish recon used as the gate electrode of an MOS transistor on this gate oxide, The process which carries out the ion implantation of the p mold impurity by using this polish recon and p mold ion-implantation resist as a mask, The process which carries out the ion implantation of the n mold impurity by using this polish recon and n mold ion-implantation resist as a mask, The manufacture approach of the electrostatic-protection equipment according to claim 12 which includes the process which forms a silicide layer in the process which forms a gate side-attachment-wall insulator in the side attachment wall of this polish recon and this gate oxide, and the front face of this n mold cathode high concentration impurity range and the front face of this p mold anode high concentration impurity range.

[Claim 14] The manufacture approach of the electrostatic-protection equipment according to claim 13

characterized by arranging the location of the photo-mask edge for p mold ion implantations on the polish recon field distant from n mold impurity impregnation field edge in the process which carries out the ion implantation of p mold according to claim 13 or the n mold impurity when n mold cathode high concentration impurity range of the trigger diode of a thyristor forms p mold substrate or p mold well, and pn junction.

[Claim 15] The manufacture approach of the electrostatic-protection equipment according to claim 13 characterized by arranging the location of the photo-mask edge for n mold ion implantations on the polish recon field distant from p mold impurity impregnation field edge in the process which carries out the ion implantation of p mold or n mold impurity of a publication to ****** 13 when p mold anode high concentration impurity range of the trigger diode of a thyristor forms n mold substrate or n mold well, and pn junction.

[Claim 16] The process which forms the isolation insulator which separates the active region in which the MOS transistor from which this insulating means formation process constitutes a semiconductor integrated circuit is formed, The process which carries out the ion implantation of the p mold impurity by using this isolation insulator and p mold ion-implantation resist as a mask, The process which carries out the ion implantation of the n mold impurity by using this isolation insulator and n mold ion-implantation resist as a mask, The manufacture approach of the electrostatic-protection equipment according to claim 12 which includes the process which forms a silicide layer in the front face of this p mold anode high concentration impurity range, and the front face of this n mold cathode high concentration impurity range.

[Claim 17] The manufacture approach of the electrostatic-protection equipment according to claim 16 characterized by arranging the location of the photo-mask edge for p mold ion implantations on the isolation insulator of the center of a trigger diode which is distant from n mold impurity impregnation field edge in the process which carries out the ion implantation of p mold according to claim 16 and the n mold impurity when n mold cathode high concentration impurity range of the trigger diode of a thyristor forms p mold substrate or p mold well, and pn junction.

[Claim 18] The manufacture approach of the electrostatic-protection equipment according to claim 16 characterized by arranging the location of the photo-mask edge for n mold ion implantations on the isolation insulator of the center of a trigger diode which is distant from p mold impurity impregnation field edge in the process which carries out the ion implantation of p mold according to claim 16 and the n mold impurity when p mold anode high concentration impurity range , n mold substrate , or n mold well of a trigger diode of a thyristor forms pn junction .

[Claim 19] The electrostatic-protection equipment which is the electrostatic-protection circuit which detours the static electricity surge which flows from the input/output terminal of a semiconductor integrated circuit to a reference voltage line, and was equipped with the trigger diode according to claim 1, It has protection diode. This electrostatic-protection equipment and this protection diode It is arranged at juxtaposition between the input-and-output signal line of this semiconductor integrated circuit, and the reference voltage line. The anode of a thyristor and the anode gate with which this electrostatic-protection equipment was equipped, and the cathode of this protection diode It connects with this input-and-output signal line. The cathode of this thyristor, the cathode gate, and the anode of this protection diode It is the electrostatic-protection circuit which is connected to this reference voltage line and is further equipped with the resistor formed into the well of the conductivity type with which this electrostatic-protection equipment differs from a substrate between this anode of this thyristor, and this cathode of this protection diode.

[Claim 20] The electrostatic-protection equipment which is the electrostatic-protection circuit which detours the static electricity surge which flows from the I/O section of a semiconductor integrated circuit to a current supply line, and was equipped with the trigger diode according to claim 1, It has the protection diode formed into n mold substrate or n mold well. This electrostatic-protection equipment and this protection diode It is arranged at juxtaposition between the input-and-output signal line of a

semiconductor integrated circuit, and the current supply line. The anode of a thyristor and the anode gate with which this electrostatic-protection equipment was equipped, and the cathode of this protection diode It connects with the current supply line of this semiconductor integrated circuit. The cathode of this thyristor, and the anode of this protection diode It connects with this input-and-output signal line. The cathode gate of this thyristor It is the electrostatic-protection circuit which is connected to this reference voltage line and is further equipped with the resistor formed into the well of the conductivity type with which this electrostatic-protection equipment differs from a substrate between this cathode of this thyristor, and this anode of this protection diode.

[Claim 21] It is the electrostatic-protection circuit which detours the static electricity surge which flows from the current supply line of a semiconductor integrated circuit to a reference voltage line. It has electrostatic-protection equipment equipped with the trigger diode according to claim 1. This electrostatic-protection equipment The anode and the anode gate of a thyristor with which are arranged between the current supply line of this semiconductor integrated circuit, and the reference voltage line, and this electrostatic-protection equipment was equipped It is the electrostatic-protection circuit where it connects with this current supply line, and the cathode and the cathode gate of this thyristor are connected to this reference voltage line.

[Claim 22] It is the electrostatic-protection circuit which is an electrostatic-protection circuit given in either of claims 19-21, and is manufactured by the manufacture approach as the manufacture approach of electrostatic-protection equipment according to claim 12 that n mold cathode high concentration impurity range of this protection diode and p mold anode high concentration impurity range are the same.

[Claim 23] The static electricity surge which flows from the input/output terminal, reference voltage terminal, or current supply terminal of a semiconductor integrated circuit It is the electrostatic-protection circuit missed to other input/output terminals, reference voltage terminals, or current supply terminals. An electrostatic-protection circuit according to claim 19, It has the electrostatic-protection circuit according to claim 20 and the electrostatic-protection circuit according to claim 21. The electrostatic-protection circuit given in this claim 19 is formed between the input-and-output signal line of this semiconductor integrated circuit, and the reference voltage line. An electrostatic-protection circuit given in this claim 20 is an electrostatic-protection circuit where it is formed between the input-and-output signal line of this semiconductor integrated circuit, and the current supply line, and the electrostatic-protection circuit according to claim 21 is formed between the current supply line of this semiconductor integrated circuit, and the reference voltage line.

[Claim 24] The static electricity surge which flows from the input/output terminal, reference voltage terminal, or current supply terminal of a semiconductor integrated circuit It is the electrostatic-protection circuit missed to other input/output terminals, reference voltage terminals, or current supply terminals. The first anode and anode gate of a thyristor with which are equipped with three electrostatic-protection equipments equipped with the trigger diode according to claim 1, and this first electrostatic-protection equipment was equipped **** on the current supply line of this semiconductor integrated circuit, and the cathode of this first thyristor is connected to the input-and-output signal line of this semiconductor integrated circuit. The cathode gate of this first thyristor is connected to the reference voltage line of this semiconductor integrated circuit. The second anode and anode gate of a thyristor with which the second electrostatic-protection equipment was equipped are connected to the input-and-output signal line of this semiconductor integrated circuit. this -- The cathode and the cathode gate of this second thyristor are connected to a reference voltage line. this -- the electrostatic-protection circuit which connects to the current supply line of this semiconductor integrated circuit the third anode and anode gate of a thyristor with which the third electrostatic-protection equipment was equipped, and connects the cathode and the cathode gate of this third thyristor to a reference voltage line.

[Claim 25] The static electricity surge which flows from the input/output terminal, reference voltage terminal, or current supply terminal of a semiconductor integrated circuit It is the electrostatic-

protection circuit missed to other input/output terminals, reference voltage terminals, or current supply terminals. An electrostatic-protection circuit according to claim 19, Have the electrostatic-protection circuit according to claim 21, and the electrostatic-protection circuit of a publication is formed in this claim 19 between the input-and-output signal line of this semiconductor integrated circuit, and the reference voltage line. The electrostatic-protection circuit where the electrostatic-protection circuit according to claim 21 is formed between the current supply line of this semiconductor integrated circuit, and the reference voltage line.

[Claim 26] The static electricity surge which flows from the input/output terminal, reference voltage terminal, or current supply terminal of a semiconductor integrated circuit It is the electrostatic-protection circuit missed to other input/output terminals, reference voltage terminals, or current supply terminals. It has the first electrostatic-protection equipment which equipped ****** 1 with the trigger diode of a publication between the reference voltage line of this semiconductor integrated circuit, and the input-and-output signal line. The first anode and anode gate of a thyristor with which the electrostatic-protection equipment of this first was equipped Connect with the input-and-output signal line of this semiconductor integrated circuit, and the cathode and the cathode gate of this first thyristor are connected to the reference voltage line of an integrated circuit this whole half-**. It has the second electrostatic-protection equipment equipped with the trigger diode according to claim 1 between the reference voltage line of this semiconductor integrated circuit, and the current supply line. this — the electrostatic-protection circuit which connects to the current supply line of this semiconductor integrated circuit the second anode and anode gate of a thyristor with which the second electrostatic-protection equipment was equipped, and connects the cathode and the cathode gate of this second thyristor to the reference voltage line of this semiconductor integrated circuit.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is set to a semiconductor integrated circuit, and relates to the electrostatic-protection circuit using the electrostatic-protection equipment protected from a semiconductor integrated circuit being destroyed by the static electricity bleedoff phenomenon from the semiconductor integrated circuit charged [which was charged and static electricity-flowed] to the exterior, its manufacture approach, and electrostatic-protection equipment from the outside.
[0002]
[Description of the Prior Art] The electrostatic discharge made into a problem with a semiconductor integrated circuit is a phenomenon which static electricity flows into a semiconductor integrated circuit from the electrified body, a machinery, etc., or the semiconductor integrated circuit itself is charged in friction etc., and emits static electricity to an external conductor at the time of the handling of a semiconductor integrated circuit. Since static electricity flows into a semiconductor integrated circuit out of an inflow or a semiconductor integrated circuit in an instant, an excessive current flows inside semiconductor integrated circuit equipment, and an excessive electrical potential difference is impressed to an internal circuitry according to an overcurrent, junction destruction, wiring fusing, oxide-film dielectric breakdown, etc. arise within a semiconductor integrated circuit, and a semiconductor integrated circuit is destroyed by the electrostatic-discharge phenomenon.
[0003] In order to prevent a semiconductor integrated circuit being destroyed by the electrostatic-discharge phenomenon, generally, electrostatic-protection equipment is formed between the external terminal of a semiconductor integrated circuit, and the internal circuitry, and the detour circuit of static electricity is formed. This electrostatic-protection equipment is formed using the production process which forms a semiconductor integrated circuit. In order not to make the manufacturing cost of a semiconductor integrated circuit increase, it is desirable to form electrostatic-protection equipment, without adding a production process special in addition to the production process of a semiconductor integrated circuit.
[0004] Generally the protection network which consists of a current-limiting component called the diffused resistor and polish recon resistance which restrict the current which flows the interior of a semiconductor integrated circuit transitionally as electrostatic-protection equipment, and electrical-potential-difference clamp components which control the electrical potential difference impressed to an internal circuitry, such as diode, a thyristor, an MOS transistor, and a bipolar transistor, is used.
[0005] The thyristor excels in passing the excessive discharge current as an electrical-potential-difference clamp component. However, the special device has been carried out in order for a semiconductor integrated circuit to be easy to be destroyed before thyristor actuation since it is originally 25-40V, and high tension, and, as for the trigger voltage from which a thyristor will be in an ON state, to carry out trigger voltage under low-battery-izing.
[0006] Drawing 24 shows the sectional view of conventional electrostatic-protection equipment. An example of the thyristor which carries out a trigger by the low battery is shown in drawing 24 (Japan

patent number No. 2505652).
[0007] With reference to drawing 24 , it is formed in p mold substrate 1 by n mold impurity diffused layer, and the slack n mold well 2 is formed. In n mold well 2, p mold anode high concentration impurity range 4 and n mold anode gate high concentration impurity range 5 are formed. p mold high concentration impurity range 55 is formed in the boundary of n mold well 2 and p mold substrate 1, a part of p mold high concentration impurity range 55 is surrounded by n mold well 2, and the part is surrounded by p mold substrate 1. n mold cathode high concentration impurity range 6 and p mold cathode gate high concentration impurity range 7 are formed in the field of p mold substrate 1 which is separated from n mold well 2. p mold anode high concentration impurity range 4 and n mold anode gate high concentration impurity range 5 are connected to the anode terminal 36 through contact 16 and metal 18. n mold cathode high concentration impurity range 6 and p mold cathode gate high concentration impurity range 7 are connected to the cathode terminal 54 through contact 16 and metal 53.
[0008] With reference to drawing 25 , the low-battery thyristor explained by drawing 19 is arranged between the current supply line of a semiconductor integrated circuit, and a reference voltage line as an example. The anode terminal 36 of electrostatic-protection equipment 56 is connected to the current supply line 52, and the cathode terminal 54 of electrostatic-protection equipment 56 is connected to the reference voltage line 45. If the overvoltage by the electrostatic discharge joins the current supply line 52 and reaches the trigger voltage of the thyristor in electrostatic-protection equipment 56, a thyristor will be turned on and a low resistance path will be formed between the current supply line 52 and the reference voltage line 45. According to this low resistance path, static electricity which flows from the current supply terminal 51 is missed to the reference voltage terminal 44, and destruction of the semiconductor integrated circuit 57 connected to the current supply line 52 and the reference voltage line 45 is prevented.
[0009] When p mold high concentration impurity range 55 is not formed, the trigger voltage of a thyristor is decided by breakdown voltage of p mold substrate 1 and n mold well 2, and turns into 40V and high tension from 25V in the production process of a common CMOS semiconductor integrated circuit. By such high tension, before a thyristor is turned on, the internal circuitry of a semiconductor integrated circuit 57 will be destroyed. The trigger voltage of a thyristor shown in drawing 24 can be decided by breakdown voltage of p mold high concentration impurity range 55 and n mold well 2, and can make breakdown voltage lower than the breakdown voltage of p mold substrate 1 and n mold well 2 by existence of p mold high concentration impurity range 55.
[0010]
[Problem(s) to be Solved by the Invention] If the minimum processing dimension of a semiconductor integrated circuit becomes detailed and high-speed operation of an integrated circuit comes to be desired, in order to reduce the source / drain diffused resistor of an MOS transistor, and gate wiring resistance, the Salicide process (self-align silicide) came to be used. At the Salicide process, after exposing the silicon substrate surface and polish recon front face which are formed into low resistance and depositing refractory metals, such as titanium and cobalt, the alloy (silicide) of silicon and a refractory metal is formed in a silicon front face and a polish recon front face by adding heat treatment.
[0011] As for the silicon front face which is not covered with the gate oxide or the isolation insulator of an MOS transistor, a silicide layer is formed at the Salicide process in a CMOS process. As for both the p mold high concentration impurity ranges 55 and silicon front faces of n mold well 2 that serve as a trigger in the thyristor by which a trigger is carried out by the low battery of drawing 20 , a silicide layer is formed. Then, p mold high concentration impurity range 55 and n mold well 2 are short-circuited electrically, and have a problem of breakdown stopping arising between p mold high concentration impurity range 55 and n mold well 2. Moreover, when p mold high concentration impurity range 55 and n mold well 2 connect too hastily electrically, while saying that n mold anode gate high concentration impurity range 5, n mold well 2, p mold high concentration impurity range 55, p mold substrate 1, and p mold cathode gate high concentration impurity range 7 connect too hastily, and the anode terminal 36

and the cathode terminal 54 short-circuit, a title arises.
[0012] As a means to avoid that p mold high concentration impurity range 55 and n mold well 2 connect too hastily electrically, the process which forms a semiconductor integrated circuit before a silicide process has the approach of forming independently the insulator which checks silicide-ization on p mold high concentration impurity range 55 and the silicon front face of the pn junction section of n mold well 2. However, by this approach, since a new process and a new photo mask will be added to the process of a semiconductor integrated circuit, there is a problem that the manufacturing cost of a semiconductor integrated circuit rises.
[0013] Even if this invention is the case where the Salicide process is used by manufacture of a semiconductor integrated circuit, it aims at offering the electrostatic-protection circuit using the electrostatic-protection equipment which can be formed without adding the process and photo mask of a semiconductor integrated circuit special to a production process in any way, its manufacture approach, and electrostatic-protection equipment.
[0014]
[Means for Solving the Problem] The electrostatic-protection equipment concerning this invention is formed in the input section or the output section of a semiconductor integrated circuit. It is electrostatic-protection equipment which protects the internal circuitry of this semiconductor integrated circuit from the inflow of the static electricity surge from the outside of this semiconductor integrated circuit to this semiconductor integrated circuit, or bleedoff of the static electricity surge to the exterior of this semiconductor integrated circuit to this semiconductor integrated circuit. It has the thyristor and the trigger diode which carries out the trigger of this thyristor to an ON state by the low battery. This trigger diode n mold cathode high concentration impurity range and p mold anode high concentration impurity range, It has an insulating means to insulate electrically the silicide layer formed in the front face of this n mold cathode high concentration impurity range, and the silicide layer formed in the front face of this p mold anode high concentration impurity range, and the above-mentioned object is attained by that.
[0015] The gate oxide which this insulating means is formed between this n mold cathode high concentration impurity range and this p mold anode high concentration impurity range, and forms the gate of the MOS transistor of this semiconductor integrated circuit, It is formed on this gate oxide at the side attachment wall of the polish recon by which patterning was carried out, and this gate oxide and this polish recon. The gate side-attachment-wall insulator with which the silicide layer formed in the front face of this n mold cathode high concentration impurity range and the silicide layer formed in the front face of this p mold anode high concentration impurity range are insulated electrically may be included.
[0016] This insulating means may contain the isolation insulator which is formed between this n mold cathode high concentration impurity range and this p mold anode high concentration impurity range, and forms the component isolation region of the MOS transistor of this semiconductor integrated circuit.
[0017] This electrostatic-protection equipment is formed in the p type semiconductor substrate, this n mold cathode high concentration impurity range is formed into n mold well, this a part of p mold anode high concentration impurity range is included in this n mold well, and these a part of other p mold anode high concentration impurity ranges may be included in this p type semiconductor substrate or p mold well.
[0018] This electrostatic-protection equipment is formed in the p type semiconductor substrate, this p mold anode high concentration impurity range is formed into this p type semiconductor substrate or p mold well, this a part of n mold cathode high concentration impurity range is included in n mold well, and these a part of other n mold cathode high concentration impurity ranges may be included in this p type semiconductor substrate or this p mold well.
[0019] This electrostatic-protection equipment is formed in the n-type-semiconductor substrate, this n mold cathode high concentration impurity range is formed into this n-type-semiconductor substrate,

this a part of p mold anode high concentration impurity range is included in p mold well, and these a part of other p mold anode high concentration impurity ranges may be included in this n-type-semiconductor substrate or n mold well.

[0020] This electrostatic-protection equipment is formed in the n-type-semiconductor substrate, this p mold anode high concentration impurity range is formed into p mold well, this a part of n mold cathode high concentration impurity range is included in this p mold well, and these a part of other n mold cathode high concentration impurity ranges may be included in this n-type-semiconductor substrate or n mold well.

[0021] The process which the manufacture approach of the electrostatic-protection equipment concerning this invention is the manufacture approach of electrostatic-protection equipment according to claim 1, and forms n mold cathode high concentration impurity range, The insulating means formation process which forms an insulating means to insulate electrically the process which forms p mold anode high concentration impurity range, and the silicide layer formed in the front face of this n mold cathode high concentration impurity range and the silicide layer formed in the front face of this p mold anode high concentration impurity range is included. The above-mentioned object is attained by that.

[0022] The process which forms the gate oxide in which this insulating means formation process forms the gate of the MOS transistor of a semiconductor integrated circuit on a silicon substrate, The process which carries out patterning of the polish recon used as the gate electrode of an MOS transistor on this gate oxide, The process which carries out the ion implantation of the p mold impurity by using this polish recon and p mold ion-implantation resist as a mask, The process which carries out the ion implantation of the n mold impurity by using this polish recon and n mold ion-implantation resist as a mask, The process which forms a silicide layer in the process which forms a gate side-attachment-wall insulator in the side attachment wall of this polish recon and this gate oxide, and the front face of this n mold cathode high concentration impurity range and the front face of this p mold anode high concentration impurity range may be included.

[0023] In the process which carries out the ion implantation of p mold according to claim 13 or the n mold impurity, when n mold cathode high concentration impurity range of the trigger diode of a thyristor forms p mold substrate or p mold well, and pn junction, the location of the photo-mask edge for p mold ion implantations may be arranged on the polish recon field distant from n mold impurity impregnation field edge.

[0024] In the process which carries out the ion implantation of p mold or n mold impurity of a publication to ****** 13, when p mold anode high concentration impurity range of the trigger diode of a thyristor forms n mold substrate or n mold well, and pn junction, the location of the photo-mask edge for n mold ion implantations may be arranged on the polish recon field distant from p mold impurity impregnation field edge.

[0025] The process which forms the isolation insulator which separates the active region in which the MOS transistor from which this insulating means formation process constitutes a semiconductor integrated circuit is formed, The process which carries out the ion implantation of the p mold impurity by using this isolation insulator and p mold ion-implantation resist as a mask, The process which forms a silicide layer in the process which carries out the ion implantation of the n mold impurity by using this isolation insulator and n mold ion-implantation resist as a mask, and the front face of this p mold anode high concentration impurity range and the front face of this n mold cathode high concentration impurity range may be included.

[0026] In the process which carries out the ion implantation of p mold according to claim 16 and the n mold impurity, when n mold cathode high concentration impurity range of the trigger diode of a thyristor forms p mold substrate or p mold well, and pn junction, the location of the photo-mask edge for p mold ion implantations may be arranged on the isolation insulator of the center of a trigger diode which is distant from n mold impurity impregnation field edge.

[0027] In the process which carries out the ion implantation of p mold according to claim 16 and the n

mold impurity, when p mold anode high concentration impurity range, n mold substrate, or n mold well of a trigger diode of a thyristor forms pn junction, the location of the photo-mask edge for n mold ion implantations may be arranged on the isolation insulator of the center of a trigger diode which is distant from p mold impurity impregnation field edge.

[0028] The electrostatic-protection equipment which the electrostatic-protection circuit concerning this invention is an electrostatic-protection circuit which detours the static electricity surge which flows from the input/output terminal of a semiconductor integrated circuit to a reference voltage line, and was equipped with the trigger diode according to claim 1, It has protection diode. This electrostatic-protection equipment and this protection diode It is arranged at juxtaposition between the input-and-output signal line of this semiconductor integrated circuit, and the reference voltage line. The anode of a thyristor and the anode gate with which this electrostatic-protection equipment was equipped, and the cathode of this protection diode It connects with this input-and-output signal line. The cathode of this thyristor, the cathode gate, and the anode of this protection diode It has further the resistor which is connected to this reference voltage line and formed into the well of the conductivity type with which this electrostatic-protection equipment differs from a substrate between this anode of this thyristor, and this cathode of this protection diode, and the above-mentioned object is attained by that.

[0029] The electrostatic-protection equipment which other electrostatic-protection circuits concerning this invention are electrostatic-protection circuits which detour the static electricity surge which flows from the I/O section of a semiconductor integrated circuit to a current supply line, and was equipped with the trigger diode according to claim 1, It has the protection diode formed into n mold substrate or n mold well. This electrostatic-protection equipment and this protection diode It is arranged at juxtaposition between the input-and-output signal line of a semiconductor integrated circuit, and the current supply line. The anode of a thyristor and the anode gate with which this electrostatic-protection equipment was equipped, and the cathode of this protection diode It connects with the current supply line of this semiconductor integrated circuit. The cathode of this thyristor, and the anode of this protection diode It connects with this input-and-output signal line. The cathode gate of this thyristor It has further the resistor which is connected to this reference voltage line and formed into the well of the conductivity type with which this electrostatic-protection equipment differs from a substrate between this cathode of this thyristor, and this anode of this protection diode, and the above-mentioned object is attained by that.

[0030] The electrostatic-protection circuit of others [pan / concerning this invention] is an electrostatic-protection circuit which detours the static electricity surge which flows from the current supply line of a semiconductor integrated circuit to a reference voltage line. It has electrostatic-protection equipment equipped with the trigger diode according to claim 1. This electrostatic-protection equipment The anode and the anode gate of a thyristor with which are arranged between the current supply line of this semiconductor integrated circuit, and the reference voltage line, and this electrostatic-protection equipment was equipped It connects with this current supply line, and the cathode and the cathode gate of this thyristor are connected to this reference voltage line, and the above-mentioned object is attained by that.

[0031] It may be manufactured by the manufacture approach as the manufacture approach of electrostatic-protection equipment according to claim 12 that n mold cathode high concentration impurity range of this protection diode and p mold anode high concentration impurity range are the same.

[0032] Other electrostatic-protection circuits to the pan concerning this invention The input/output terminal of a semiconductor integrated circuit, It is the electrostatic-protection circuit which misses the static electricity surge which flows from a reference voltage terminal or a current supply terminal to other input/output terminals, reference voltage terminals, or current supply terminals. An electrostatic-protection circuit according to claim 19, It has the electrostatic-protection circuit according to claim 20 and the electrostatic-protection circuit according to claim 21. The electrostatic-protection circuit given in this claim 19 is formed between the input-and-output signal line of this semiconductor integrated

circuit, and the reference voltage line. The electrostatic-protection circuit given in this claim 20 is formed between the input-and-output signal line of this semiconductor integrated circuit, and the current supply line, an electrostatic-protection circuit according to claim 21 is formed between the current supply line of this semiconductor integrated circuit, and a reference voltage line, and the above-mentioned object is attained by that.

[0033] Other electrostatic-protection circuits to the pan concerning this invention The input/output terminal of a semiconductor integrated circuit, The static electricity surge which flows from a reference voltage terminal or a current supply terminal Other input/output terminals, It is the electrostatic-protection circuit missed to a reference voltage terminal or a current supply terminal. The first anode and anode gate of a thyristor with which are equipped with three electrostatic-protection equipments equipped with the trigger diode according to claim 1, and this first electrostatic-protection equipment was equipped **** on the current supply line of this semiconductor integrated circuit, and the cathode of this first thyristor is connected to the input-and-output signal line of this semiconductor integrated circuit. The cathode gate of this first thyristor is connected to the reference voltage line of this semiconductor integrated circuit. The second anode and anode gate of a thyristor with which the second electrostatic-protection equipment was equipped are connected to the input-and-output signal line of this semiconductor integrated circuit. this — The cathode and the cathode gate of this second thyristor are connected to a reference voltage line. this — the third anode and anode gate of a thyristor with which the third electrostatic-protection equipment was equipped are connected to the current supply line of this semiconductor integrated circuit, the cathode and the cathode gate of this third thyristor are connected to a reference voltage line, and the above-mentioned object is attained by that.

[0034] Other electrostatic-protection circuits to the pan concerning this invention The input/output terminal of a semiconductor integrated circuit, It is the electrostatic-protection circuit which misses the static electricity surge which flows from a reference voltage terminal or a current supply terminal to other input/output terminals, reference voltage terminals, or current supply terminals. An electrostatic-protection circuit according to claim 19, Have the electrostatic-protection circuit according to claim 21, and the electrostatic-protection circuit of a publication is formed in this claim 19 between the input-and-output signal line of this semiconductor integrated circuit, and the reference voltage line. An electrostatic-protection circuit according to claim 21 is formed between the current supply line of this semiconductor integrated circuit, and a reference voltage line, and the above-mentioned object is attained by that.

[0035] Other electrostatic-protection circuits to the pan concerning this invention The input/output terminal of a semiconductor integrated circuit, The static electricity surge which flows from a reference voltage terminal or a current supply terminal Other input/output terminals, It is the electrostatic-protection circuit missed to a reference voltage terminal or a current supply terminal. It has the first electrostatic-protection equipment which equipped ****** 1 with the trigger diode of a publication between the reference voltage line of this semiconductor integrated circuit, and the input-and-output signal line. The first anode and anode gate of a thyristor with which the electrostatic-protection equipment of this first was equipped Connect with the input-and-output signal line of this semiconductor integrated circuit, and the cathode and the cathode gate of this first thyristor are connected to the reference voltage line of an integrated circuit this whole half-**. It has the second electrostatic-protection equipment equipped with the trigger diode according to claim 1 between the reference voltage line of this semiconductor integrated circuit, and the current supply line. this — the second anode and anode gate of a thyristor with which the second electrostatic-protection equipment was equipped are connected to the current supply line of this semiconductor integrated circuit, the cathode and the cathode gate of this second thyristor are connected to the reference voltage line of this semiconductor integrated circuit, and the above-mentioned object is attained by that.

[0036]

[Embodiment of the Invention] Hereafter, this invention is explained to a detail based on the gestalt of

operation.
[0037] Although the gestalt of operation of this invention explains the example using the p type semiconductor which contained low-concentration boron in the semi-conductor substrate, of course, the following explanation is applicable with the semi-conductor substrate and n-type-semiconductor substrate containing other impurities.
[0038] Drawing 1 is a sectional view explaining the structure of the thyristor which has the trigger diode which is the gestalt of the 1 operation by this invention, and is electrostatic-protection equipment.
[0039] n mold well 2 is formed into p mold substrate 1. p mold cathode gate high concentration impurity range 7 and n mold cathode high concentration impurity range 6 are formed in the front face of p mold substrate 2 which is separated from n mold well 2 on which p mold anode high concentration impurity range 4 and n mold anode gate high concentration impurity range 5 are formed in the front face of n mold well 2. The silicide layer 10 is formed in each front face of p mold anode high concentration impurity range 4, n mold anode gate high concentration impurity range 5, p mold cathode gate high concentration impurity range 7, and n mold KANODO high concentration impurity range 6, and it has connected with metal 17, 18, and 19 through contact 16.
[0040] The trigger diode A which gives the trigger of thyristor actuation consists of a p mold high concentration impurity range 8 used as the anode of a trigger diode A, an n mold high concentration impurity range 9 used as a cathode, and an n mold well 2. The gate oxide 13 which constitutes the gate part of the MOS transistor of a semiconductor integrated circuit, the polish recon 14, and the gate side-attachment-wall insulator 12 exist in the upper part of p mold high concentration impurity range 8 used as the anode of a trigger diode A, and n mold high concentration impurity range 9 used as a cathode. On PO ** silicon 14, the silicide layer 11 formed simultaneously with the silicide layer 10 on silicon at the Salicide process of a semiconductor integrated circuit is. Since a silicide layer is not formed in the front face of the gate side-attachment-wall insulator 12, n mold high concentration impurity range 9 used as p mold high concentration impurity range 8 of a trigger diode A and a cathode does not connect too hastily by the silicide layer.
[0041] When it is a thyristor without a trigger diode A, the trigger electrical potential difference of thyristor actuation is decided by breakdown voltage between n mold well 2 and p mold substrate 1, and, generally turns into high tension of 40 volts from 25 volts in the production process of a CMOS semiconductor integrated circuit. On the other hand, since the trigger electrical potential difference of the thyristor by this invention is decided by breakdown voltage of p mold high concentration impurity range 8 of a trigger diode, and n mold well, it can form the thyristor which will be in an ON state by the low battery.
[0042] Drawing 2 shows the sectional view of other examples of the electrostatic-protection equipment concerning the gestalt of operation of this invention. With the thyristor structure of drawing 2 , the isolation insulator 3 of the MOS transistor of a semiconductor integrated circuit exists between p mold high concentration impurity range 8 used as the anode of a trigger diode A, and n mold high concentration impurity range 9 used as a cathode. Since the silicide layer 10 is not formed in the isolation insulator 3, p mold high concentration impurity range 8 of a trigger diode and n mold high concentration impurity range 9 used as a cathode have structure which is not short-circuited by formation of a silicide layer.
[0043] Drawing 3 shows the sectional view of the example of further others of the electrostatic-protection equipment concerning the gestalt of operation of this invention. Although the example of drawing 1 and drawing 2 showed the structure of the electrostatic-protection equipment which makes breakdown between p mold high concentration impurity range 8 used as the anode of a trigger diode A, and n mold well 2 the trigger of thyristor actuation Also according to the structure which makes a trigger n mold high concentration impurity range 9 used as the cathode of a trigger diode, and breakdown of one between p substrates and which shows in drawing 3 A trigger can be carried out by the low battery and the thyristor structure which the anode and cathode of a trigger diode A do not

short-circuit by formation of a silicide layer can be given. In drawing 3 , it has the structure where a part of n mold high concentration impurity range 9 used as the cathode of a trigger diode is included in p mold substrate 1, and a part is included in n mold well 2.

[0044] Drawing 4 shows the sectional view of the example of further others of the electrostatic-protection equipment concerning the gestalt of operation of this invention. Generally in manufacture of a CMOS semiconductor integrated circuit, p mold well with high impurity concentration [high concentration / substrate / 1 / p mold / in addition to the field of n mold well 2 on p mold substrate 1] is formed. Drawing 4 is the example in which p mold well 20 was formed to the gestalt of operation of drawing 1 . Also in the structure of drawing 4 , the thyristor which carries out a trigger by the low battery is obtained.

[0045] Hereafter, with reference to drawing 11 , the manufacture approach of the electrostatic-protection equipment by this invention of drawing 1 is explained from drawing 5 . Drawing 10 shows main process sectional views from drawing 5 . Drawing 11 shows the flow chart showing the production process of electrostatic-protection equipment.

[0046] Drawing 5 shows the sectional view showing the process which forms the isolation insulator 3. Drawing 6 shows the sectional view showing the process which forms n mold well 2. Drawing 7 shows the sectional view showing the process which forms the gate side-attachment-wall insulator 12. Drawing 8 shows the sectional view showing the process which carries out patterning of the photoresist 26. Drawing 9 shows the sectional view showing the process which deposits a refractory metal 27. Drawing 10 shows the sectional view showing the process which forms the silicide layers 10 and 11.

[0047] Although the process illustrated here corresponds to manufacture of the electrostatic-protection equipment of drawing 1 , it can be manufactured at the process same as the electrostatic-protection equipment of drawing 2 . It is because what is necessary is just to form the isolation insulator 3 instead of forming the same structure as the gate section of an MOS transistor in the trigger diode section A with the electrostatic-protection equipment of drawing 2 .

[0048] With reference to drawing 11 and drawing 5 - drawing 10 , first, as shown in drawing 5 , the isolation insulator 3 is formed in p mold substrate 1 (S101). Although the approach by local oxidation treatment (local oxidation of silicon;LOCOS) of silicon and the approach by shallow trench (sharrow trench isolation) formation are generally used as the formation approach of the isolation insulator 3, what kind of approach may be used. The thin oxide film 22 covers the field which is not [divided] with the isolation insulator 3.

[0049] Next, as shown in drawing 6 , a photoresist is applied all over a wafer, using n mold well formation photo mask, according to a photolithography process, patterning of Foto Regis ** 21 for n mold well impregnation is carried out, and n mold impurity is poured in. p mold impurity may be poured in using p mold well impregnation mask for p mold well formation after this. A photoresist is removed, heat treatment is added, n mold impurity is diffused, and n mold well 2 is formed (S102).

[0050] Next, as shown in drawing 7 , the thin oxide film 22 is removed by etching, and the gate oxide 13 of an MOS transistor is formed on a silicon substrate by oxidation treatment (S103). After making polish recon deposit all over a wafer and applying a photoresist to the whole surface, using a gate formation photo mask, patterning of the resist for the gates is carried out at a photolithography process, and patterning of the polish recon 14 is carried out on gate oxide 13 by polish recon etching (S104). A photoresist is removed, to an acid chemically-modified degree, a thin oxide film is grown up into the whole surface, a photoresist is applied all over a wafer, using the LDD impregnation mask of an NMOS transistor, patterning of the resist for LDD impregnation of an NMOS transistor is carried out, and n mold impurity is poured into the source / drain field of an NMOS transistor according to a photoresist process (S105). Simultaneously, in order to control the short channel effect of an NMOS transistor, p mold impurity may be poured in. An impurity may be poured into drawing 1 or n mold anode gate high concentration impurity range 5 of the electrostatic-protection equipment of drawing 2 , n mold cathode high concentration impurity range 6, and n mold high concentration impurity range 9 at this time.

[0051] A photoresist is removed and a photoresist is again applied to the whole surface. Using the LDD impregnation mask of a PMOS transistor, according to a photoresist process, patterning of the resist for LDD impregnation of a PMOS transistor is carried out, and p mold impurity is poured into the source / drain field of a PMOS transistor (S106). Simultaneously, in order to control the short channel effect of a PMOS transistor, n mold impurity may be poured in. An impurity may be poured into drawing 1 or p mold high concentration impurity range 4 of the electrostatic-protection equipment of drawing 2 , p mold cathode gate high concentration impurity range 7, and p mold high concentration impurity range 8 at this time.

[0052] A photoresist is removed, an oxide film is deposited on the whole surface, and the gate side-attachment-wall insulator 12 is formed in the side attachment wall of the polish recon 14 by carrying out anisotropy oxide film etching of the whole surface (S107). The thin oxide films 24 and 25 are deposited and a photoresist is applied to the whole surface. Using the source / drain impregnation mask of an NMOS transistor, according to a photoresist process, patterning of the photoresist 23 the source / for drain impregnation of an NMOS transistor is carried out, and n mold impurity is poured in. n mold impurity is poured into n mold anode gate high concentration impurity range 5, n mold cathode high concentration impurity range 6, and n mold high concentration impurity range 9 at this process (S108). A photoresist is removed and a photoresist is applied to the whole surface.

[0053] As shown in drawing 8 , using the source / drain impregnation mask of a PMOS transistor, according to a photoresist process, patterning of the photoresist 26 the source / for drain impregnation of a PMOS transistor is carried out, and p mold impurity is poured in (S110). p mold impurity is poured into drawing 1 or p mold anode high concentration impurity range 4 of the electrostatic-protection equipment of drawing 2 , p mold cathode gate high concentration impurity range 7, and p mold high concentration impurity range 8 at this process (S109).

[0054] As shown in drawing 9 , a photoresist is removed, the oxide film on the active region of silicon and the oxide film on the top face of polish recon are removed, and a refractory metal 27 is deposited (S110).

[0055] As shown in drawing 10 , heat treatment is added and the silicide layers 10 and 11 are formed in the front face of a silicon substrate, and the front face of the polish recon 14, respectively, and it is foil ****** (S111) about an unreacted refractory metal. A silicide layer is not formed in the front face of the isolation insulator 3, and the front face of the gate side-attachment-wall insulator 12. Since a silicide layer is not formed in the gate side-attachment-wall insulator 12, p mold high concentration impurity range 8 and n mold high concentration impurity range 9 which constitute a trigger diode are not short-circuited electrically. Then, a layer insulation object is deposited on the whole surface, and carries out flattening, a photoresist is applied to the whole surface and patterning of the resist for contact hole openings is carried out using a contact hole formation photo mask. Etch a layer insulation object, carry out opening of the contact hole, and metal is made to deposit all over a wafer, and using the photo mask for metal, if patterning of metal is performed, formation of drawing 1 or the electrostatic-protection equipment of drawing 2 will be completed.

[0056] The layout location of a photo mask at the time of pouring an impurity into p mold high concentration impurity range and n mold high concentration impurity range which constitute the trigger diode of the electrostatic-protection equipment by this invention from drawing 12 using drawing 14 hereafter is explained. Although the layout location explained here supports the trigger diode section of electrostatic-protection equipment, it is applicable also to manufacture of the protection diode which constitutes the below-mentioned electrostatic-protection circuit.

[0057] Drawing 12 shows the sectional view explaining the nonconformity of the production process which should be avoided at the time of formation of the electrostatic-protection equipment concerning the gestalt of operation of this invention. This sectional view is a sectional view which extracted and expanded the trigger diode section A of the electrostatic-protection equipment of drawing 1 . n mold high concentration impurity is poured into a part of p mold high concentration impurity range 8 which is

the anode of a trigger diode, and n mold impurity range 9a is formed in it. This is because the photo-mask edge was set as the location 28 by the side of an anode for the NMOS source / photo mask for drain impregnation rather than the edge 29 of a lifting and the gate polish recon 14 in the alignment gap on the occasion of the source / drain impregnation of the NMOS transistor of a semiconductor integrated circuit. If it is high concentration even when n mold high impurity concentration is slighter than p mold high impurity concentration, n mold impurity range 9a will be formed. At the Salicide process, since, as for p mold high concentration impurity range 8 and the front face of n mold impurity range 9a, the silicide layer 10 is formed, p mold high concentration impurity range 8 and n mold impurity range 9a will be short-circuited electrically. Since n mold impurity range 9a, n mold well 2, and n mold impurity range 9 are the same conductivity types, the anode and cathode of a trigger diode short-circuit. When a cathode connects with an anode too hastily, the anode gate and the cathode gate of a thyristor which are electrostatic-protection equipment containing about [that hard flow breakdown of a trigger diode stops arising] and a trigger diode will connect too hastily, leakage current will usually arise from the anode gate in high potential to the cathode gate in a reference potential, and the normal operation of a semiconductor integrated circuit will be checked.

[0058] Drawing 13 shows the sectional view showing the formation approach of the electrostatic-protection equipment concerning the gestalt of operation of this invention. This sectional view is a sectional view which explains the layout location of the NMOS source / photo mask for drain impregnation about the good case where a short circuit way is not formed between the anode of a trigger diode, and a cathode. In the production process of a semiconductor integrated circuit, only the distance DMAX which causes the greatest alignment gap arranges [the NMOS source / photo mask for drain impregnation] the location 30 of the photo-mask edge the NMOS source / for drain impregnation on the polish recon field by the side of a cathode to gate polish recon to the gate polish recon edge 29 which is an impurity impregnation field edge. It is avoidable that n mold high concentration impurity is poured into an anode side with this.

[0059] In addition, it also sets in the manufacture process of the protection diode formed into n mold substrate later mentioned by drawing 16 , or n mold well. Can apply this layout technique and, in the case of the structure where the anode and cathode of a trigger diode are insulated with the isolation insulator 3 like drawing 2 Only the distance which causes the greatest alignment gap for the NMOS source / photo mask for drain impregnation to an isolation insulator should arrange the location 30 of the photo-mask edge the NMOS source / for drain impregnation to the cathode side to the component isolation region insulator edge.

[0060] Drawing 14 is drawing which makes a trigger breakdown of n mold high concentration impurity range 9 used as the cathode of a trigger diode, and p mold substrate 1 and which extracted and expanded the trigger diode section of the electrostatic-protection equipment of drawing 3 . If p mold high concentration impurity is poured into n mold high concentration impurity range 9 which is a cathode at the time of the PMOS source / drain impregnation, even when p mold high impurity concentration is slighter than n mold high impurity concentration, when high, p mold impurity range will be formed in the gate 14 side of n mold high concentration impurity range 9. Then, by the silicide layer, n mold high concentration impurity range 9, and p mold substrate 1 and p mold high concentration impurity range 8 will connect too hastily, and the anode and cathode of a trigger diode will short-circuit.

[0061] Drawing 14 shows the sectional view showing the formation approach of other examples of the electrostatic-protection equipment concerning the gestalt of operation of this invention. This sectional view is a sectional view explaining the anode of a trigger diode, and the location of the PMOS source / photo mask for drain impregnation with which a short circuit way is not formed between cathodes.

[0062] In the production process of a semiconductor integrated circuit, when only the distance DMAX from which the PMOS source / photo mask for drain impregnation starts the greatest alignment gap to the polish recon 14 arranges the location 34 of the photo-mask edge the PMOS source / for drain impregnation on the polish recon field by the side of a cathode to the gate polish recon edge 33 which is

an impurity impregnation field edge, it is avoidable that p mold high concentration impurity is poured into a cathode side. This layout technique is applicable also to the manufacture process of the protection diode of drawing 15 formed into p mold substrate or p mold well. Moreover, in the case of the trigger diode structure where the anode and cathode of a trigger diode are electrically insulated like drawing 2 using the isolation insulator 3, only the distance DMAX which causes the greatest alignment gap for the PMOS source / photo mask for drain impregnation to the isolation insulator 3 should arrange the location 34 of the photo-mask edge the PMOS source / for drain impregnation at the anode side to the edge of the isolation insulator 3 which is an impurity impregnation field edge.

[0063] Drawing 15 , drawing 18 , and drawing 19 are the examples of the electrostatic-protection circuit which consists of electrostatic-protection equipment according to claim 1, and explain the detail.

[0064] Drawing 15 shows the mimetic diagram showing the electrostatic-protection circuit which consists of electrostatic-protection equipment concerning the gestalt of operation of this invention. This mimetic diagram shows the example which used the electrostatic-protection equipment indicated to claim 1 between the input-and-output signal line and the reference voltage line, and constituted the electrostatic-protection circuit.

[0065] The electrostatic-protection circuit consists of electrostatic-protection equipment 39 according to claim 1, protection diode 41, and a well resistor 46. It connects with the input-and-output signal line 43, and the anode terminal 36 of electrostatic-protection equipment connects the cathode terminal 37 and the cathode gate terminal 38 to the reference voltage line 45. Between an input-and-output signal line and a reference voltage line, semiconductor integrated circuit 40a which should be protected from static electricity connects. The well resistor 46 is formed by n mold well, when a semi-conductor substrate is p mold, and when a semi-conductor substrate is n mold, it can be formed by p well. The protection diode 41 consists of p mold anode high concentration impurity ranges 8 and n mold cathode high concentration impurity ranges 9 which were formed by the same production process as electrostatic-protection equipment 39, and were formed into p mold or n mold well.

[0066] Drawing 16 shows the sectional view showing the structure of the protection diode which constitutes the electrostatic-protection circuit of this invention. Drawing 17 shows the sectional view showing the structure of other examples of the protection diode which constitutes the electrostatic-protection circuit of this invention. Drawing 16 and drawing 17 show the example of structure of the protection diode 41 formed on p mold substrate 1. Also in the protection diode 41, the anode and the cathode as well as the trigger diode of electrostatic-protection equipment are insulated using the gate structure which consists of a gate side-attachment-wall insulator 12, gate oxide 13, and polish recon 14 so that p mold anode high concentration impurity range 8 and n mold cathode high concentration impurity range 9 may not connect too hastily in a silicide layer. Like the trigger diode A of drawing 2 , even if the insulation with p mold anode high concentration impurity range 8 and n mold cathode high concentration impurity range 9 uses the isolation insulator 3, it is possible. It connects with the input-and-output signal line 43, and an anode 8 connects n mold cathode high concentration impurity range 9 of the protection diode 41 to the reference voltage line 45.

[0067] In the electrostatic-protection circuit of drawing 15 , when forward static electricity has flowed into the input-and-output terminal 42, breakdown arises in the PN junction of the protection diode 41, and a breakdown current flows to the protection diode 41. If a breakdown current flows to the protection diode 41, since the anode terminal 36 will become high tension by the well resistor 46, rather than the breakdown voltage of the protection diode 41, slightly large electrostatic-protection equipment 39 carries out a turn-on, the detour of low resistance is formed between the input-and-output signal line 43 and the reference voltage line 45, and a turn-on electrical potential difference can miss static electricity which flows from the input-and-output terminal 42 on the reference voltage line 45 through electrostatic-protection equipment 39. Moreover, since the diode formed in p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39, p mold substrate 1, n mold well 2, and n mold anode gate high concentration impurity range 5 serves as the forward direction and the

protection diode 41 also serves as the forward direction when forward static electricity flows from the reference voltage terminal 44, forward static electricity which flows from the reference voltage terminal 44 can be missed to the input–and–output signal line 43 and an input/output terminal 42.
[0068] Drawing 18 shows the mimetic diagram showing other examples of the electrostatic–protection circuit which consists of electrostatic–protection equipment concerning the gestalt of operation of this invention. This mimetic diagram is a mimetic diagram showing the example which constituted the electrostatic–protection circuit between an electrical–potential–difference supply line and an input–and–output signal line using the electrostatic–protection equipment indicated to claim 1.
[0069] The electrostatic–protection circuit consists of electrostatic–protection equipment 39 according to claim 1, protection diode 41, and a well resistor 46. The anode terminal 36 of electrostatic–protection equipment is connected to the current supply line 52, the cathode terminal 37 is connected to the input–and–output signal line 43, and the cathode gate terminal 38 is connected to the reference voltage line 45. Between the current supply line 52 and the input–and–output signal line 43, semiconductor integrated circuit 40b which should be protected from static electricity is connected.
[0070] The protection diode 41 consists of p mold anode high concentration impurity ranges 8 and n mold cathode high concentration impurity ranges 9 which were formed by the same production process as electrostatic–protection equipment 39, and were formed into n mold well. Drawing 17 is the example of structure of the protection diode 41 formed in n mold well 2 on p mold substrate 1. n mold cathode high concentration impurity range 9 of the protection diode 41 is connected to the current supply line 52, and p mold anode high concentration impurity range 8 is connected to the input–and–output signal line 43.
[0071] In the electrostatic–protection circuit of drawing 18 , when forward static electricity flows into the current supply terminal 51, reverse voltage is impressed to the PN junction of the protection diode 41, breakdown arises, and a breakdown current flows to the protection diode 41. If a breakdown current flows to the protection diode 41, since the anode terminal 36 will become high tension by the well resistor 46, electrostatic–protection equipment 39 carries out a turn–on, the detour of low resistance is formed between the current supply line 52 and the input–and–output signal line 43, and static electricity which flows from the current supply terminal 51 can be missed to the input–and–output signal line 43 through electrostatic–protection equipment 39. Moreover, since the protection diode 41 serves as the forward direction when forward electrostatic charge flows from the input–and–output terminal 42, forward static electricity which flows from the input–and–output terminal 42 can be detoured to the current supply line 52.
[0072] Drawing 19 is drawing showing the example which constituted the electrostatic–protection circuit between an electrical–potential–difference supply line and a reference voltage line using the electrostatic–protection equipment indicated to claim 1.
[0073] The anode terminal 36 of electrostatic–protection equipment is connected to the current supply line 52, and the cathode terminal 37 and the cathode gate terminal 38 are connected to the reference voltage line 45. Between the current supply line 52 and the reference voltage line 45, semiconductor integrated circuit 40c which should be protected from static electricity is connected.
[0074] In the electrostatic–protection circuit of drawing 19 , when forward electrostatic charge has flowed into the current supply terminal 51, reverse voltage is impressed to the trigger diode of electrostatic–protection equipment 39, electrostatic–protection equipment 39 carries out a turn–on, the detour of low resistance is formed between the current supply line 52 and the reference voltage line 45, and the electrostatic charge which flows from the current supply terminal 51 can be missed to the reference voltage line 45 through electrostatic–protection equipment 39. Moreover, since the diode formed in p mold cathode gate high concentration impurity range 7 of electrostatic–protection equipment, p mold substrate 1, n mold well 2, and n mold anode gate high concentration impurity range 5 becomes the forward direction when forward static electricity flows from the reference voltage terminal 44, forward static electricity which flows from the reference voltage terminal 44 can be detoured to the

current supply line 52 and the current supply terminal 51.
[0075] Drawing 20 is drawing showing the example of the electrostatic-protection circuit which constituted the circuit which can detour static electricity among all the terminal pairs of the input/output terminal of a semiconductor integrated circuit, a current supply terminal, and a reference voltage terminal using the electrostatic-protection equipment indicated to claim 1.
[0076] an electrostatic-protection circuit — the electrostatic-protection equipments 39a, 39b, and 39c according to claim 1, the protection diodes 41a and 41b, and a well — it consists of resistors 46. Anode terminal 36of electrostatic-protection equipment 39a a was connected to the current supply line 52, cathode terminal 37a was connected to the input-and-output signal line 43, and cathode gate terminal 38a is connected to the reference voltage line 45. Anode terminal 36of electrostatic-protection equipment 39b b was connected to the input-and-output signal line 43, and cathode terminal 37b and cathode gate terminal 38b are connected to the reference voltage line 45. Anode terminal 36of electrostatic-protection equipment 39c c was connected to the current supply line 52, and cathode terminal 37c and cathode gate terminal 38c are connected to the reference voltage line 45. Between the current supply line 52 and the reference voltage line 45, 40d of semiconductor integrated circuits which should be protected from static electricity has connected. The protection diodes 41a and 41b are formed by the same production process as the electrostatic-protection equipments 39a, 39b, and 39c. The protection diode on p mold substrate 1 which protection diode 41a consists of a p mold anode high concentration impurity range 8 and an n mold cathode high concentration impurity range 9, and is shown in drawing 17 formed in the well 2 n mold is an example of 1 structure. It connected with the input-and-output signal line 43, and p mold anode high concentration impurity range 8 of protection diode 41a has connected n mold cathode high concentration impurity range 9 to the current supply line 52. The protection diode formed on p mold substrate 1 which protection diode 41b consists of a p mold anode high concentration impurity range and an n mold cathode high concentration impurity range 9, and is shown in drawing 16 is an example of 1 structure. It connected with the reference voltage line 45, and p mold anode high concentration impurity range 8 of protection diode 41b has connected n mold cathode high concentration impurity range 9 to the input-and-output signal line 43.
[0077] if reverse voltage is impressed to the PN junction of protection diode 41a and a reverse current flows to diode 41a in the electrostatic-protection circuit of drawing 20 , when forward static electricity flows into the current supply terminal 51 — a well — by the resistor 46 Since anode terminal 36a becomes high tension to cathode terminal 37a Electrostatic-protection equipment 39a carries out a turn-on, the detour of low resistance is formed between the current supply line 52 and the input-and-output signal line 43, and static electricity which flows from the current supply line 52 can be missed to the input-and-output signal line 43 through electrostatic-protection equipment 39a. Moreover, when forward static electricity flows from an input-and-output signal line, protection diode 41a can become the forward direction, and can detour forward static electricity which flows from the input-and-output terminal 42 to the current supply line 52. Moreover, when forward static electricity has flowed into the input-and-output terminal 42, reverse voltage is impressed by the PN junction of protection diode 41b. moreover, the thing which protection diode 41a becomes the forward direction, and a current flows to protection diode 41a or 41b — a well, since anode terminal 36b becomes high tension from cathode terminal 37b by the resistor 46 Electrostatic-protection equipment 39a carries out a turn-on, the detour of low resistance is formed between the input-and-output terminal 43 and the reference voltage line 45, and static electricity which flows from the input-and-output terminal 42 can be missed on the reference voltage line 45 through electrostatic-protection equipment 39b. Since p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39b, p mold substrate 1, and the diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5 serve as the forward direction and protection diode 41b also becomes the forward direction when forward static electricity flows from the reference voltage terminal 44, it can let the detour of the low resistance by forward static electricity which flows from the reference voltage terminal 44 pass, and can miss to the

input–and–output signal line 43. Moreover, when forward static electricity has flowed into the current supply terminal 51, a current supply line becomes high tension to a reference supply line, electrostatic–protection equipment 39c carries out a turn–on, the detour of low resistance is formed between the current supply line 52 and the reference voltage line 45, and static electricity which flows from a current supply terminal can be missed to the reference voltage line 45 through electrostatic–protection equipment 39c. Moreover, when forward static electricity flows from the reference voltage terminal 44 p mold cathode gate high concentration impurity range 7 of electrostatic–protection equipment 39c, p mold substrate 1, and DAIO 1 DO formed n molds in a well 2 and n mold anode gate high concentration impurity range 5 become the forward direction. Moreover, since the protection diodes 41a and 41b are connected with a serial in the forward direction, forward static electricity which flows from the reference voltage terminal 44 can be missed through the detour of low resistance to the current supply line 52 and the current supply terminal 51.

[0078] Drawing 21 is drawing showing other examples which constituted the electrostatic–protection circuit which can detour static electricity among all the terminal pairs between the input–and–output terminal of a semiconductor integrated circuit, a current supply terminal, and a reference voltage terminal using the electrostatic–protection equipment indicated to claim 1.

[0079] Drawing 21 serves as an electrostatic–protection circuit which excluded the protection diodes 41a and 41b in the electrostatic–protection circuit of a publication to drawing 20 . Although the electrical potential difference more than the breakdown voltage of the protection diodes 41a and 41b may be impressed to 40d of semiconductor integrated circuits at 40d of semiconductor integrated circuits when forward static electricity flows from the input–and–output terminal 42 by omitting the protection diodes 41a and 41b When 40d of semiconductor integrated circuits is not destroyed to electrical–potential–difference impression of turn–on electrical–potential–difference extent of the electrostatic–protection equipments 39a and 39b By using the electrostatic–protection circuit of a publication for drawing 21 , the electrostatic–protection circuit which can detour static electricity can be constituted among all the terminals between the input–and–output terminal of a semiconductor integrated circuit, a current supply terminal, and a reference voltage terminal so that it may describe below.

[0080] When making a current supply terminal bypass forward static electricity which flows from the input–and–output terminal 42 by drawing 21 The input–and–output signal line 43 from the input–and–output terminal 42, electrostatic–protection equipment 39b, The reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic–protection equipment 39c, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, The detour of static electricity of the low resistance said to the current supply terminal 51 through the current supply line 52 is formed. Moreover, when making the reference voltage terminal 44 bypass forward static electricity which flows from the input–and–output terminal 42 by drawing 22 , the detour of static electricity of the low resistance said to the reference voltage terminal 44 through the input–and–output signal line 43, electrostatic–protection equipment 39b, and the reference voltage line 45 is formed from the input–and–output terminal 42. Moreover, when making the input–and–output terminal 42 bypass forward static electricity which flows from the current supply terminal 51 by drawing 21 , the detour of static electricity of the low resistance said to the input–and–output signal terminal 42 through the current supply terminal 51, the current supply line 52, electrostatic–protection equipment 39a, and the input–and–output signal line 43 is formed. Moreover, when detouring forward static electricity which flows from the current supply terminal 51 to the reference voltage terminal 44 by drawing 21 , the detour of static electricity of the low resistance said to the reference voltage terminal 44 through the current supply terminal 51, the current supply line 52, electrostatic–protection equipment 39c, and the reference voltage line 45 is formed. Moreover, when detouring forward static electricity which flows from the reference voltage terminal 44 to the input–and–output terminal 42 by drawing 21 , the detour of static electricity of low resistance called the reference

voltage terminal 44, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39b, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, the input-and-output signal line 43, and the input-and-output terminal 42 is formed. Furthermore, when detouring forward static electricity which flows from the reference voltage terminal 44 to the current supply terminal 51 by drawing 21 , the detour of static electricity of the low resistance formed with the reference voltage terminal 44, the reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39c, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, the current supply line 52, and the current supply terminal 51 is formed. In the electrostatic-protection circuit of drawing 21 , since the layout area of an electrostatic-protection circuit can be reduced by the abbreviation of protection diode and the chip area in which a semiconductor integrated circuit is formed can be reduced when 40d of semiconductor integrated circuits is not destroyed to the electrical-potential-difference impression more than the breakdown voltage of the protection diodes 41a and 41b, the number of the chips of the semiconductor integrated circuit made on a wafer increases, and there is effectiveness which the cost of the chip of a semiconductor integrated circuit reduces. a well — although resistance 46 is what restricts static electricity which flows into 40d of semiconductor integrated circuits — the static electricity resistance of 40d of semiconductor integrated circuits — responding — a well — it is also possible to omit resistance 46.

[0081] Drawing 22 is drawing showing other examples which constituted the electrostatic-protection circuit which can detour static electricity among all the terminal pairs between the input-and-output terminal of a semiconductor integrated circuit, a current supply terminal, and a reference voltage terminal using the electrostatic-protection equipment indicated to claim 1.

[0082] In drawing 22 , it is electrostatic-protection circuitry which excluded electrostatic-protection equipment 39a and protection diode 41a in the electrostatic-protection circuit given in drawing 20 .

[0083] Also in the drawing 22 electrostatic-protection circuit, the electrostatic-protection circuit which can detour static electricity among all the terminals between the input-and-output terminal of a semiconductor integrated circuit, a current supply terminal, and a reference voltage terminal is formed so that it may describe below.

[0084] When making a current supply terminal bypass forward static electricity which flows from the input-and-output terminal 42 by drawing 22 The input-and-output signal line 43 from the input-and-output terminal 42, electrostatic-protection equipment 39b, The reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39c, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, The detour of static electricity of the low resistance said to the current supply terminal 51 through the current supply line 52 is formed. Moreover, when making the reference voltage terminal 44 bypass forward static electricity which flows from the input-and-output terminal 42 by drawing 22 , the detour of static electricity of the low resistance said to the reference voltage terminal 44 through the input-and-output signal line 43, electrostatic-protection equipment 39b, and the reference voltage line 45 is formed from the input-and-output terminal 42. Moreover, when making the input-and-output terminal 42 bypass forward static electricity which flows from the current supply terminal 51 by drawing 22 The current supply terminal 51, the current supply line 52, electrostatic-protection equipment 39c, p mold cathode gate high concentration impurity range 7 of the reference voltage line 45, protection diode 41b, and electrostatic-protection equipment 39b, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, The detour of static electricity of the low resistance said to the input-and-output signal terminal 42 through the input-and-output signal line 43 is formed. Moreover, when detouring forward static electricity which flows from the current supply terminal 51 to the reference voltage terminal 44 by drawing 22 , the detour of static electricity of the low resistance said to the reference

voltage terminal 44 through the current supply terminal 51, the current supply line 52, electrostatic-protection equipment 39c, and the reference voltage line 45 is formed. Moreover, when detouring forward static electricity which flows from the reference voltage terminal 44 to the input-and-output terminal 42 by drawing 22 The reference voltage terminal 44, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39b, p mold substrate 1, and the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, The detour of static electricity of low resistance called protection diode 41b, the input-and-output signal line 43, and the input-and-output terminal 42 is formed. Furthermore, when detouring forward static electricity which flows from the reference voltage terminal 44 to the current supply terminal 51 by drawing 22 , the detour of static electricity of the low resistance formed with the reference voltage terminal 44, the reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39c, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, the current supply line 52, and the current supply terminal 51 is formed.

[0085] It compares with the electrostatic-protection circuit of drawing 20 in the electrostatic-protection circuit of drawing 22 . Between the contacts 59 of the contact 58 with the current supply line 52, and the input-and-output signal line 43 of 40d of semiconductor integrated circuits of 40d of semiconductor integrated circuits Although short-time impression of the overvoltage more than the breakdown voltage of protection diode 41a may be carried out at 40d of semiconductor integrated circuits When there is sufficient resistance to the overvoltage of the short time 40d of whose semiconductor integrated circuits is turn-on electrical-potential-difference extent of electrostatic-protection equipment 39b or static electricity **** equipment 39c, By omitting electrostatic-protection equipment 39a of drawing 20 , and protection diode 41a, the layout area of an electrostatic-protection circuit can be reduced, the chip area in which a semiconductor integrated circuit is formed can be reduced, and there is effectiveness which the cost of the chip of a semiconductor integrated circuit reduces. a well — although resistance 46 is what restricts static electricity which flows into 40d of semiconductor integrated circuits — the static electricity resistance of 40d of semiconductor integrated circuits — responding — a well — it is also possible to omit resistance 46.

[0086] Drawing 23 is drawing showing other examples which constituted the electrostatic-protection circuit which can detour static electricity among all the terminal pairs between the input-and-output terminal of a semiconductor integrated circuit, a current supply terminal, and a reference voltage terminal using the electrostatic-protection equipment indicated to claim 1.

[0087] In drawing 23 , it is electrostatic-protection circuitry which excluded protection diode 41b in the electrostatic-protection circuit of a publication to drawing 22 .

[0088] When making a current supply terminal bypass forward static electricity which flows from the input-and-output terminal 42 by drawing 23 The input-and-output terminal 42 ON / output signal line 43, electrostatic-protection equipment 39b, The reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39c, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, The detour of static electricity of the low resistance said to the current supply terminal 51 through the current supply line 52 is formed. Moreover, when making the reference voltage terminal 44 bypass forward static electricity which flows from the input-and-output terminal 42 by drawing 23 , the detour of static electricity of the low resistance said to the reference voltage terminal 44 through the input-and-output signal line 43, electrostatic-protection equipment 39b, and the reference voltage line 45 is formed from the input-and-output terminal 42. Moreover, when making the input-and-output terminal 42 bypass forward static electricity which flows from the current supply terminal 51 by drawing 23 The current supply terminal 51, the current supply line 52, electrostatic-protection equipment 39c, the reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39b, p mold substrate 1, the forward direction diode formed n molds in a well 2 and

n mold anode gate high concentration impurity range 5, The detour of static electricity of the low resistance said to the input-and-output signal 42 through the input-and-output signal line 43 is formed. Moreover, when detouring forward static electricity which flows from the current supply terminal 51 to the reference voltage terminal 44 by drawing 23 , the detour of static electricity of the low resistance said to the reference voltage terminal 44 through the current supply terminal 51, the current supply line 52, electrostatic-protection equipment 39c, and the reference voltage line 45 is formed. Moreover, when detouring forward static electricity which flows from the reference voltage terminal 44 to the input-and-output terminal 42 by drawing 23 , the detour of static electricity of low resistance called the reference voltage terminal 44, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39b, p mold substrate 1, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, the input-and-output signal line 43, and the input-and-output terminal 42 is formed. Furthermore, when detouring forward static electricity which flows from the reference voltage terminal 44 to the current supply terminal 51 by drawing 23 , the detour of static electricity of the low resistance formed with the reference voltage terminal 44, the reference voltage line 45, p mold cathode gate high concentration impurity range 7 of electrostatic-protection equipment 39c, p mold substrate r, the forward direction diode formed n molds in a well 2 and n mold anode gate high concentration impurity range 5, the current supply line 52, and the current supply terminal 51 is formed.

[0089] It compares with the electrostatic-protection circuit of drawing 22 in the electrostatic-protection circuit of drawing 23 . Between the contacts 59 of the contact 60 with the reference voltage line 45, and the input-and-output signal line 43 of 40d of semiconductor integrated circuits of 40d of semiconductor integrated circuits Although short-time impression of the overvoltage more than the PUREKU down electrical potential difference of protection diode 41a may be carried out at 40d of semiconductor integrated circuits When there is sufficient resistance to the overvoltage of the short time 40d of whose semiconductor integrated circuits is turn-on electrical-potential-difference extent of electrostatic-protection equipment 39b, The layout area of an electrostatic-protection circuit can be reduced by the abbreviation of protection diode 41b of drawing 22 , the chip area in which a semiconductor integrated circuit is formed can be reduced, and there is effectiveness which the cost of the chip of a semiconductor integrated circuit reduces. a well — although resistance 46 is what restricts static electricity which flows into 40d of semiconductor integrated circuits — the static electricity resistance of 40d of semiconductor integrated circuits — responding — a well — it is also possible to omit resistance 46.

[0090]

[Effect of the Invention] If the thyristor structure equipped with the trigger diode by this invention is used, the electrostatic-protection equipment turned on by the low battery below the breakdown voltage of n mold well, p mold substrate (or p mold well), or p mold well and n mold substrate (or n mold well) can be formed, and more tolerant electrostatic-protection equipment can be obtained to destruction of the semiconductor integrated circuit by the electrostatic-discharge phenomenon. Moreover, p mold high concentration impurity range and n mold high concentration impurity range which constitute a trigger diode from a production process of a semiconductor integrated circuit even when the Salicide process is used are insulated electrically, and the problem that the anode and cathode of a thyristor short-circuit electrically and actuation of a semiconductor integrated circuit is checked can be avoided.

[0091] Moreover, in manufacture of a trigger diode or protection diode, if the layout technique of p mold high concentration ion implantation by this invention or n mold high concentration ion-implantation mask is used, when the Salicide process will be used by the production process of a semiconductor integrated circuit, the cathode and anode of diode can short-circuit electrically and the problem that leakage current arises in a semiconductor integrated circuit can be avoided.

[0092] Electrostatic-protection equipment can be manufactured without making the manufacturing cost of a semiconductor integrated circuit increase without adding a special process and a special photo

mask in any way, even if a silicide process is used by the production process of a semiconductor integrated circuit if the manufacture approach of trigger diode formation of the thyristor by this invention is used.

[0093] If the electrostatic-protection circuit containing the electrostatic-protection equipment of this invention is used, between a current supply line, between input-and-output signal lines and a reference voltage line, and an input-and-output signal line, and between a current supply line and a reference voltage line, the detour of static electricity can be formed and the semiconductor integrated circuit connected between a current supply line, between input-and-output signal lines and a reference voltage line, and an input-and-output signal line and between a current supply line and a reference voltage line can be protected from destruction by the electrostatic-discharge phenomenon.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the sectional view of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 2] It is the sectional view of other examples of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 3] It is the sectional view of the example of further others of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 4] It is the sectional view of the example of further others of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 5] It is a sectional view showing the process which forms the isolation insulator 3 in the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 6] It is a sectional view showing the process which forms n mold well 2 in the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 7] After forming the gate side-attachment-wall insulator 12 in the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention, it is a sectional view showing the process which pours in n mold impurity.
[Drawing 8] After carrying out patterning of the photoresist 26 in the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention, it is a sectional view showing the process which pours in a P type impurity.
[Drawing 9] It is a sectional view showing the process which deposits a refractory metal 27 in the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 10] After forming the silicide layers 10 and 11 in the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention, it is a sectional view showing the process which puts on an unreacted refractory metal and which **(ed).
[Drawing 11] It is a flow chart showing the production process of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 12] It is a sectional view explaining the nonconformity of the production process which should be avoided at the time of formation of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 13] It is the sectional view showing the formation approach of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 14] It is the sectional view showing the formation approach of other examples of the electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 15] It is a mimetic diagram showing the electrostatic-protection circuit which consists of electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 16] It is a sectional view showing the structure of the protection diode which constitutes the

electrostatic-protection circuit of this invention.
[Drawing 17] It is a sectional view showing the structure of other examples of the protection diode which constitutes the electrostatic-protection circuit of this invention.
[Drawing 18] It is a mimetic diagram showing other examples of the electrostatic-protection circuit which consists of electrostatic-protection equipment concerning the gestalt of operation of this invention.
[Drawing 19] It is a mimetic diagram showing the example of further others of the electrostatic-protection circuit concerning the gestalt of operation of this invention.
[Drawing 20] It is a mimetic diagram showing an example of the electrostatic-protection circuit concerning the gestalt of operation of this invention.
[Drawing 21] It is a mimetic diagram showing an example of the electrostatic-protection circuit concerning the gestalt of operation of this invention.
[Drawing 22] It is a mimetic diagram showing an example of the electrostatic-protection circuit concerning the gestalt of operation of this invention.
[Drawing 23] It is a mimetic diagram showing an example of the electrostatic-protection circuit concerning the gestalt of operation of this invention.
[Drawing 24] It is the sectional view of conventional electrostatic-protection equipment.
[Drawing 25] It is the mimetic diagram of the electrostatic-protection circuit which consists of conventional electrostatic-protection equipment.
[Description of Notations]
1 P Mold Substrate
2 N Mold Well
3 Isolation Insulator
4 P Mold Anode High Concentration Impurity Range
5 N Mold Anode Gate High Concentration Impurity Range
6 N Mold Cathode High Concentration Impurity Range
7 P Mold Cathode Gate High Concentration Impurity Range
8 P Mold High Concentration Impurity Range
9 N Mold High Concentration Impurity Range
10 Silicide Layer Formed on Silicon Substrate
11 Silicide Layer Formed on Polish Recon
12 Gate Side-Attachment-Wall Insulator
13 Gate Oxide
14 Polish Recon
15 Layer Insulation Object
16 Contact
17 Metal
18 Metal
19 Metal
20 P Mold Well
21 Photoresist
22 Thin Oxide Film
23 Photoresist
24 Thin Oxide Film
25 Thin Oxide Film
26 Photoresist
27 Refractory Metal Deposit
28 Location of Photo-Mask Edge NMOS Source / for Drain Impregnation
29 Gate Polish Recon Edge

30 Location of Photo-Mask Edge NMOS Source / for Drain Impregnation
32 PN Junction
33 Gate Polish Recon Edge
34 Location of Photo-Mask Edge PMOS Source / for Drain Impregnation
35 PN Junction
36 Anode Terminal of Electrostatic-Protection Equipment (Thyristor)
37 Cathode Terminal of Electrostatic-Protection Equipment (Thyristor)
38 Cathode Gate Terminal of Electrostatic-Protection Equipment (Thyristor)
39 Electrostatic-Protection Equipment
40a, 40b, 40c Semiconductor integrated circuit
41 Protection Diode
42 Input/output Terminal
43 Input-and-Output Signal Line
44 Reference Voltage Terminal
45 Reference Voltage Line
46 Well Resistor
47 Cathode Terminal
48 Anode Terminal
49 Anode Terminal
50 Cathode Terminal
51 Current Supply Terminal
52 Current Supply Line
53 Metal
54 Cathode Terminal
55 P Mold High Concentration Impurity Range
56 Electrostatic-Protection Equipment
57 Semiconductor Integrated Circuit
36a, 36b, 36c Anode terminal of electrostatic-protection equipment (thyristor)
37a, 37b, 37c Cathode terminal of electrostatic-protection equipment (thyristor)
38a, 38b, 38c Cathode gate terminal of electrostatic-protection equipment (thyristor)
39a, 39b, 39c Electrostatic-protection circuit
40d Semiconductor integrated circuit
41a, 41b Protection diode
58 Contact of Semiconductor Integrated Circuit and Current Supply Line
59 Contact of Semiconductor Integrated Circuit and Input-and-Output Signal Line
60 Contact of Semiconductor Integrated Circuit and Reference Signal Line

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[Translation done.]